Simulation and Modeling to Enhance Performance of Multicore Processor Systems

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Details of Project

Collaboration among UTEP, NMSU, and Stanford University as a part of AHP CRC TA4, HPC Enabling Technologies and Advanced Algorithmic Development

Critical Army Challenges:
Given the new era of “pervasive parallelism”, computing systems and advanced algorithm capabilities need to be developed

Army Mission Impact:
Efficient and reliable HPC libraries and computational tools will have a significant impact on the engineering and scientific communities of the Army and DoD.

Key TA4 Projects:
• Stream programming for High Performance Computing
• Simulation and Modeling to Enhance Performance of Multicore Processor Systems
• High Performance Optimization Library
• Flexible Architecture Machine
• Hybrid Optimization Schemes for Parameter Estimation Problems

Projects at The University of Texas-El Paso:
1. Simulation and Modeling to Enhance Performance of Multicore Processor Systems
2. Hybrid Optimization Schemes for Parameter Estimation Problems
3. Education and Outreach

PART 1: Performance of Simultaneous Multithreaded (SMT) Processor

Goal:
Improve Simultaneous Multithreaded (SMT) processor throughput using hardware thread priorities and SMT mode.

Questions investigated:
Are equal priorities good?

Which application pairs?

Which SMT priorities? Single-Threaded?

Simultaneous Multithreading (SMT)
Two or more threads simultaneously execute independent instruction streams, potentially doubling throughput.

Two SMT threads potentially double the computing power.

SMT System with Two Hardware Threads

Future Work

We plan to extend our SMT research in the following directions:
• Validate models using other benchmarks, in particular DoD benchmarks
• Improve model accuracy
• Extend the methodology to dynamic adaptation
• Include cache interference behavior into the Monte Carlo simulation
• Use analytical modeling tools to investigate tradeoffs leading to improved performance or productivity in multicore systems

Current and Future Work

Work In Progress

• Extend Monte Carlo processor modeling methodology to model
  (a) Out-of-order processors (targeting the Opteron)
  (b) Communication between multicores
• Build Niagara 2 Monte Carlo model
• Investigate use of GPUs for general-purpose computation
• Gather application characteristics for DoD HPCMC FY-07

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