Software-Defined Phase-Locked Loop (PLL) for Reliable Telecommunications

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Phase-Locked Loops (PLLs) are essential for precise synchronization in telecommunications systems. Traditional PLLs often rely on external timing references, such as GPS signals, which can be unreliable or unavailable. The goal is to achieve a software-defined, GPS (E1 line) non-dependent implementation of a physical PLL for where a reliable GPS signal is not available. As an alternative for starting from scratch, we are modifying the source code of DAHDI, this functions as a basement for synchronization between DAHDI itself and external systems, particularly those using the osmo-e1d protocol.

The key steps involved in this research are:

1. **DAHDI Environment Setup:** Configuring a Linux machine with DAHDI compiled from the Osmocom repository, utilizing its internal software timer.
2. **Tool Installation:** Installing necessary tools like user-space DAHDI tools and ntpd.
3. **Core Timer Accuracy Assessment:** Evaluating the core timer's accuracy using dahdi_test.
4. **DAHDI Source Code Analysis:** Analyzing the source code of dahdi_test and the coretimer_func to understand its operation.
5. **DAHDI Core Timer Modification:** Adding a new "fudge" field to the core timer structure for programmable time adjustments.
6. **Fudge Functionality Implementation:** Modifying the coretimer_func and related functions to incorporate the fudge value, enabling controlled adjustments to timing intervals.
7. **Fudge Functionality Testing:** Testing the modified DAHDI with various fudge values to verify its impact on timing.
8. **Ioctl Command Addition:** Adding new ioctl commands to DAHDI for setting and getting the fudge value from user-space applications.
9. **User-Space Tool Creation:** Developing user-space tools, including dahdi_fudge, to interact with the ioctl commands.
10. **Integration with osmo-e1d:** Modifying osmo-e1d to monitor its FIFO length and adjust the fudge value in DAHDI to maintain synchronization.

This research is significant as it addresses the limitations of traditional PLLs, which often rely on external timing references like GPS signals. By implementing this programmable PLL, we aim to provide an efficient solution for situations where precise timing is critical, and GPS (or other physical timing sync tools) signals are unreliable. This research contributes to the development of more resilient and adaptable telecommunications systems.